BP6830

3-Phase 40V P/N MOS Pre-driver with LDO

Description

The BP6830 is a three-phase 40V, high speed pre-diver for power P/N MOSFET. It has two inputs for high side and low side, and two outputs per channel with internal dead time to avoid cross-conduction.

The input logic level is compatible with 3.3V/5V/15V signal. Output 10V gate voltage for both PMOS and NMOS.

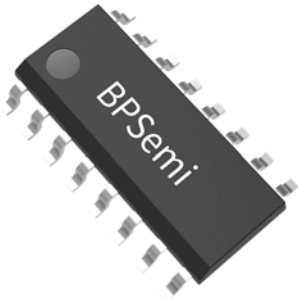
It also built in a 5V/40mA LDO for MCU or other device power supply, and have thermal shut down protection for safety.

Features

- Three-phase outputs for P/N MOS half-bridge
- Operation supply range from 8V to 40V
- Independent input for high side and low side
- Output 10V V_{GS} for both PMOS and NMOS
- 3.3V, 5V and 15V input logic compatible
- Built-in 5V/40mA LDO
- Built-in dead time
- Built-in TSD
- Available in ESOP16 package

Applications

- H-bridge
- Inverter



Typical Application

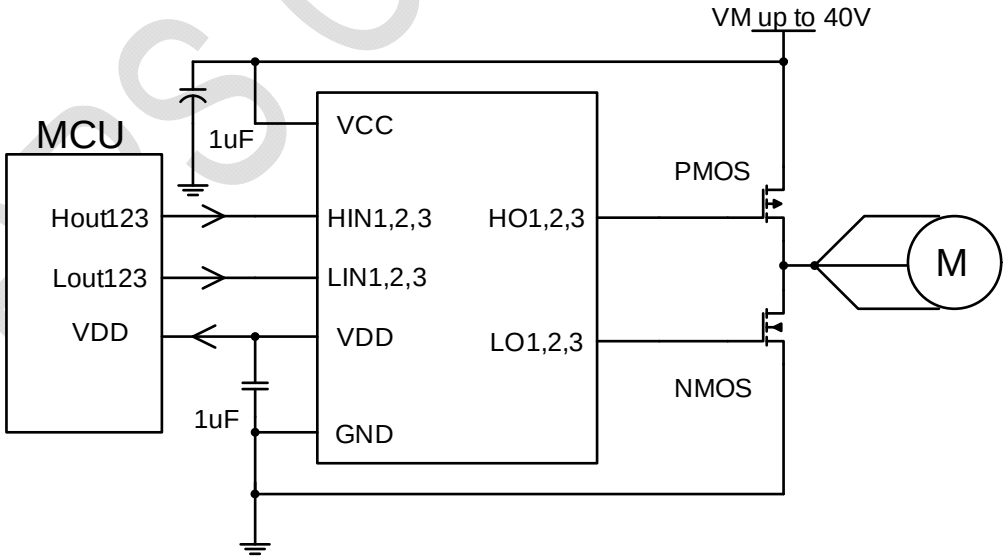


Figure 1. Schematic Diagram

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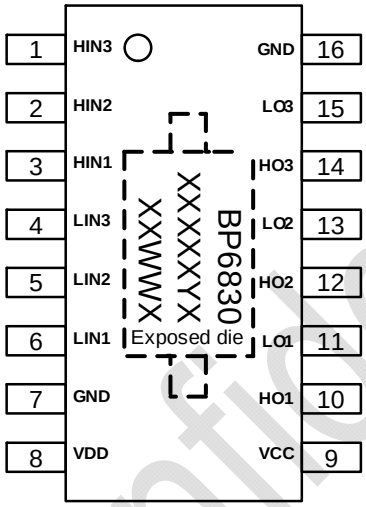
Ordering Information

Part Number	Package	Package Method	Marking
BP6830	ESOP16	Tape 3,000 pcs/Reel	BP6830 XXXXXYX XXWWX

Pin Configuration and Marking Information



XXXXXYX: Lot Code
XX: Fab code
WW: Week
X: Special code

Figure2 : Pin configuration

Pin Definition

Pin No.	Name	Description
1	HIN3	Logic input for high side channel 3
2	HIN2	Logic input for high side channel 2
3	HIN1	Logic input for high side channel 1
4	LIN3	Logic input for low side channel 3
5	LIN2	Logic input for low side channel 2
6	LIN1	Logic input for low side channel 1
7	GND	Ground, short to pin 16 internally
8	VDD	5V LDO reference output, 1uF bypass cap to ground
9	VCC	Power supply voltage, bypass cap to ground
10	HO1	High side driver output channel 1
11	LO1	Low side driver output channel 1
12	HO2	High side driver output channel 2
13	LO2	Low side driver output channel 2
14	HO3	High side driver output channel 3
15	LO3	Low side driver output channel 3
16	GND	Ground, short to pin 7 internally
	Exposed Pad	Not connect internally, suggest connecting to ground as PCB heat sink

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Absolute Maximum Ratings (Note 1)

Symbol	Parameters	Range	Units
V_{CC}	Power supply voltage	-0.3 ~ 40	V
V_{DD}	LDO output voltage	-0.3 ~ 6	V
I_{VDD}	LDO output current	-0.3 ~ 50	mA
V_{IN}	Input voltage (V_{HIN}, V_{LIN})	-0.3 ~ 20	V
V_{HO}	High side output voltage	V_{CC} -15 ~ V_{CC}	V
V_{LO}	Low side output voltage	-0.3 ~ 15	V
P_{DMAX}	Package power dissipation (note 2)	1.4	W
θ_{JA}	Thermal resistance, junction to ambient	89	°C/W
θ_{Jc}	Thermal resistance, junction to case	40	°C/W
T_J	Junction temperature	-40 ~ 150	°C
T_{STG}	Storage temperature	-55 ~ 150	°C

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. Under "recommended operating conditions" the device operation is assured, but some particular parameter may not be achieved. The electrical characteristics table defines the operation range of the device, the electrical characteristics is assured on DC and AC voltage by test program. For the parameters without minimum and maximum value in the EC table, the typical value defines the operation range, the accuracy is not guaranteed by spec.

Note 2: The maximum power dissipation decrease if temperature rise, it is decided by TJMAX, θJA, and environment temperature (TA). The maximum power dissipation is the lower one between PDMAX = (TJMAX – TA) /θJA and the number listed in the maximum table.

Recommended Operation Conditions

Symbol	Parameters	Range	Units
V_{CC}	Power supply voltage	10 ~ 28	V
I_{VDD}	LDO output current (V_{CC}=10V~28V)	0 ~ 35	mA
C_{VDD}	VDD bypass capacity	0.47 ~ 2.2	uF
$V_{IN(ON)}$	Input ON Threshold Voltage	2.9 ~ V_{CC}	V
$V_{IN(OFF)}$	Input OFF Threshold Voltage	0 ~ 0.4	V
T_{DEAD}	MCU input dead time	＞ 0.5	us
F_{PWM}	PWM Switching Frequency	50	kHZ

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Electrical Characteristics (Notes 3) (Unless otherwise specified, V_{CC}= 24V and T_A=25 °C)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Electrical Characteristics						
V_{CC_ON}	V_{CC} under voltage rising threshold		5.8	6.5	7.4	V
V_{CC_UVLO}	V_{CC} under voltage falling threshold		5.4	6.0	6.8	V
V_{CC_HYS}	V_{CC} under voltage hysteresis voltage		0.3	0.5	0.8	V
I_{QCC}	Quiescent V_{CC} supply current	V_{IN}=0V	0.3	0.5	1.0	mA
V_{DD}	VDD output voltage		4.7	5.0	5.3	V
V_{IH}	Logic “1” input trigger voltage		2.2	-	-	V
V_{IL}	Logic “0” input trigger voltage		-	-	0.6	V
$I_{ISOURCE}$	Logic “1” input bias current	V_{IN}=5V	-	32	100	uA
I_{ISINK}	Logic “0” input bias current	V_{IN}=0V	-	-	1.0	uA
V_{HO}	HO output voltage	H_{IN}=5V	VCC-11	VCC-9.5	VCC-8	V
V_{LO}	LO output voltage	L_{IN}=5V	8.5	10	11.5	V
I_{HO+}	PMOS turn-on current	H_O=V_{CC}	-	35	-	mA
I_{HO-}	PMOS turn-off current	H_O=V_{CC}-10V	-	300	-	mA
I_{LO+}	NMOS turn-on current	L_O=0V	-	60	-	mA
I_{LO-}	NMOS turn-off current	L_O=10V	-	300	-	mA
T_{SD}	TSD Temperature		-	150	-	°C
$T_{RECOVER}$	TSD release temperature		-	135	-	°C
Dynamic Characteristics (Note4)						
t_{on}	Turn-on propagation delay		-	80	-	ns
t_{off}	Turn-off propagation delay		-	30	-	ns
t_{Hr}	HO rise time		-	50	-	ns
t_{Hf}	HO fall time		-	400	-	ns
t_{Lr}	LO rise time		-	200	-	ns
t_{Lf}	LO fall time		-	50	-	ns
DT	Dead time		-	100	-	ns

Note 3: The maximum and minimum parameters specified are guaranteed by test, the typical value are guaranteed by design, characterization and statistical analysis.

Note 4: All dynamic electrical characteristics are related to PCB layout.

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Internal Block Diagram

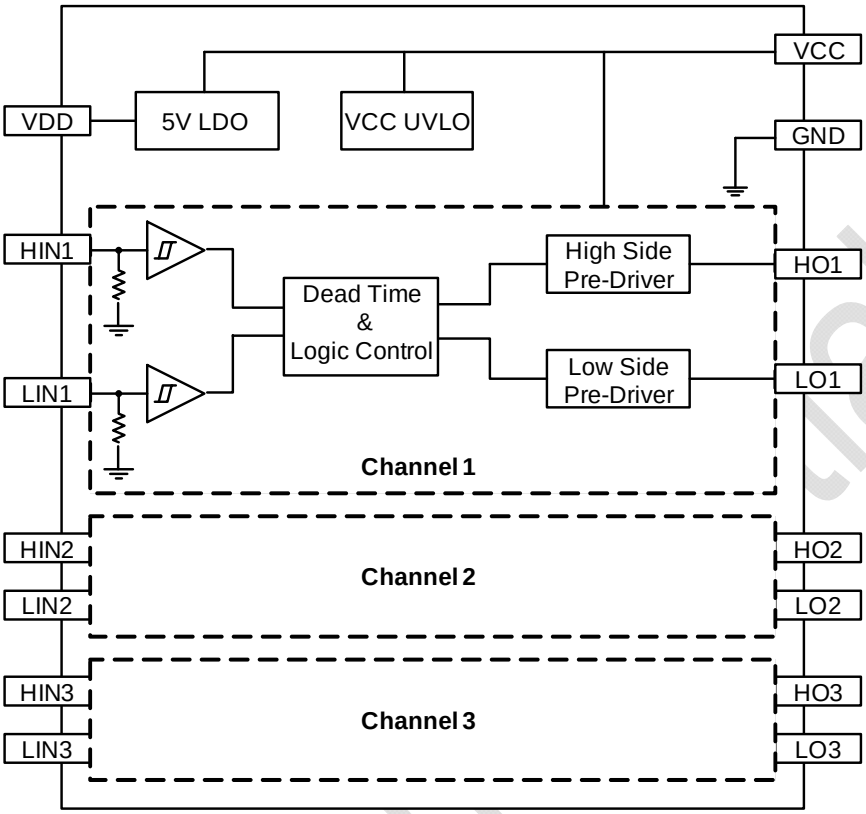

Figure3 : Internal block diagram

True Table

HIN	LIN	UVLO/TSD	HO	LO
0	0	0	OFF	OFF
0	1	0	OFF	ON
1	0	0	ON	OFF
1	1	0	OFF	OFF
X	X	1	OFF	OFF

Note:

1) X=Don't Care, 1=High, 0=Low

2) HO: ON=VCC-10V, OFF=VCC; LO: ON=10V, OFF=0V

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Waveforms

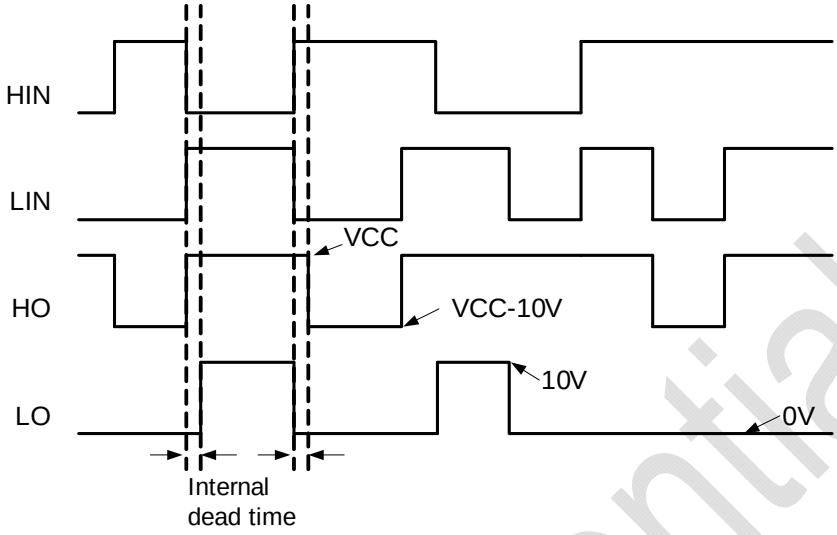

Figure 4. Input/ Output Timing Diagram

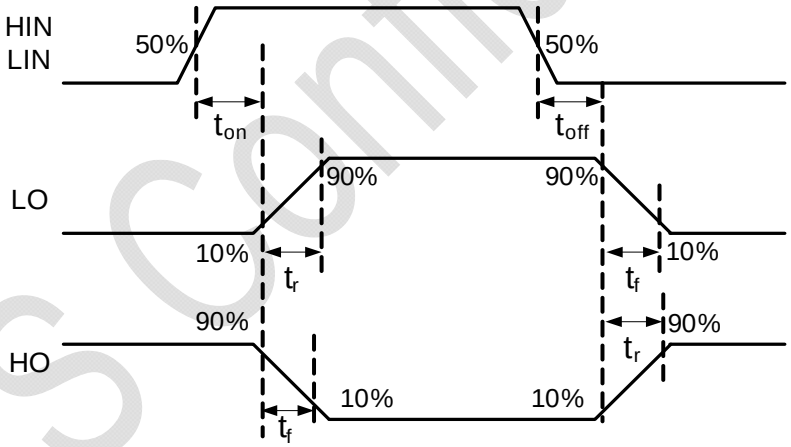

Figure 5. Switching Timing Waveforms

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Application Information

The BP6830 integrating a 5V LDO, is a P/N MOS driver and built-in under-voltage protection and thermal shut down protection.

1.Start Up

After system powered on, when the VCC pin voltage reaches the turn on threshold, the internal circuits start working. Output of LDO raises gradually, until it is steady at 5V.

2.TSD

Once the temperature is more than 150°C，the chip will shut down all outputs except LDO. When it is below 135°C，the chip recovers to normal operating station.

3.MOS drive

In general, BP6830 can drive most of P/N MOS directly. Sometimes it is necessary to add appropriate MOS gate resistant.

If capacitive load is less than 250pF, there is more than 1V overshoot voltage.

4.Input and output

BP6830 is built-in dead time, so that it cannot turn on PMOS and NMOS at the same time. The input pins only identify above 200ns pulse width.

5.PCB Layouts

Firstly, bypass capacity of VCC and VDD must be placed next to the pin as close as possible and both of 1uF value is recommended.

Secondly, exposed pad could define as ground and use for heat sink. Double panel layout should follow the way of figure 6 as below.

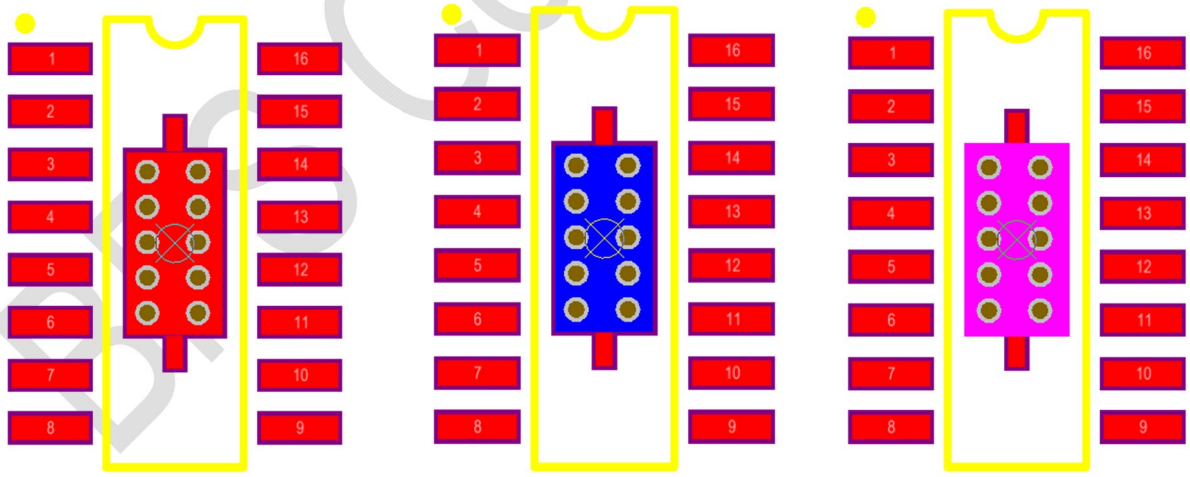

Figure 6. Exposed Pad PCB Footprint

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Typical Performance Characteristics

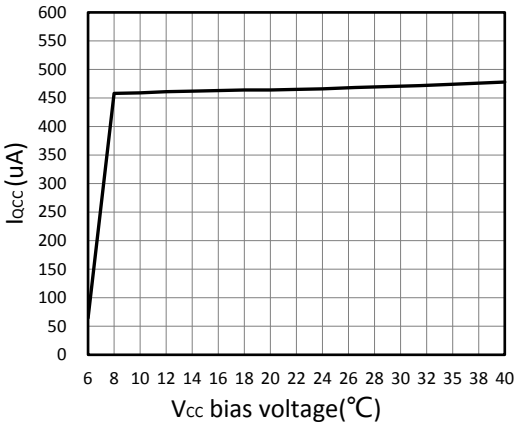

Figure 7 I_{QCC} vs. V_{CC}

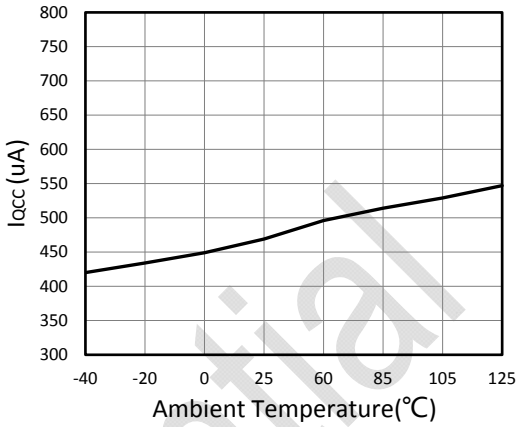

Figure 8 I_{QCC} vs. Temperature

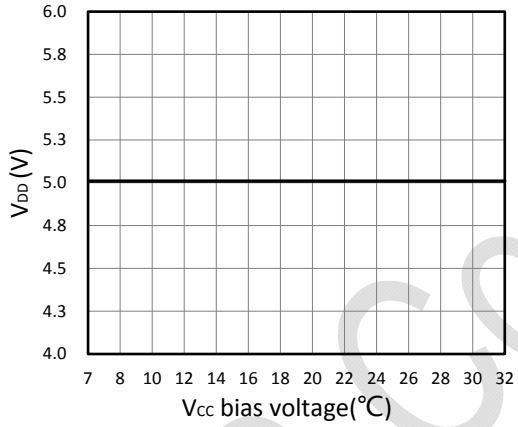

Figure 9 V_{DD} vs. V_{CC}

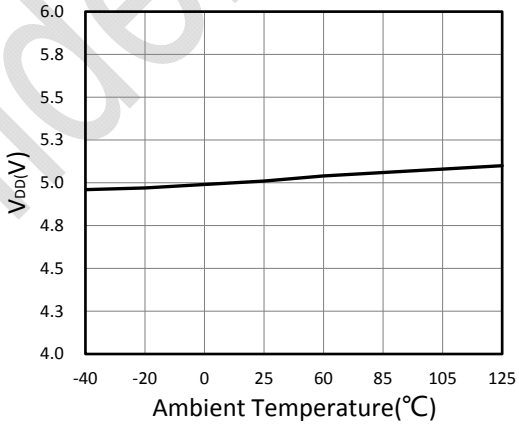

Figure 10 V_{DD} vs. Temperature

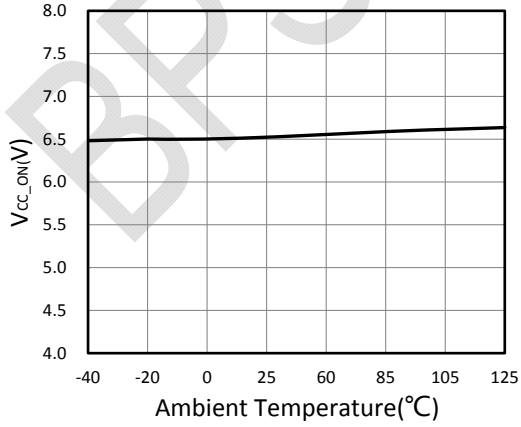

Figure 11 V_{CC_ON} vs. Temperature

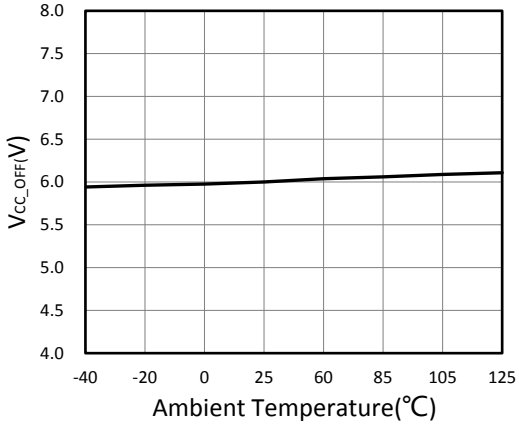

Figure 12 V_{CC_OFF} vs. Temperature

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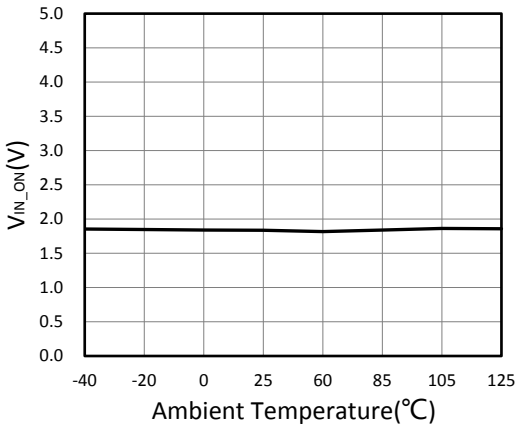

Figure 13 V_{IN_ON} vs. Temperature

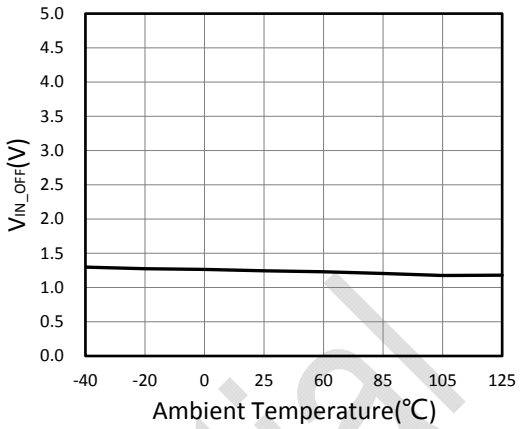

Figure 14 V_{IN_OFF} vs. Temperature

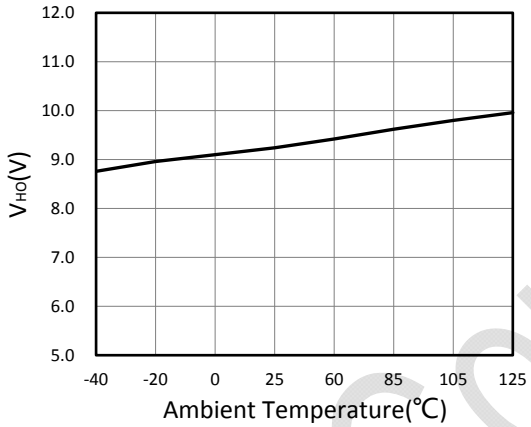

Figure 15 V_{HO} vs. Temperature

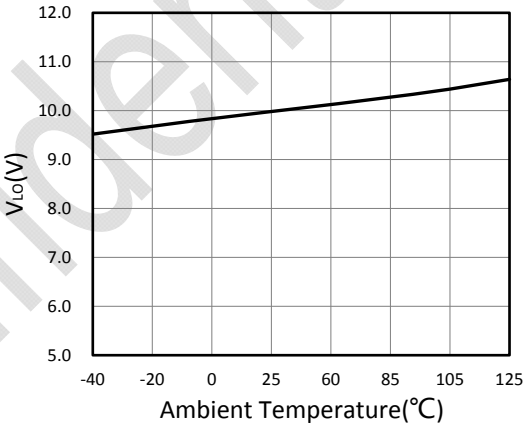

Figure 16 V_{LO} vs. Temperature

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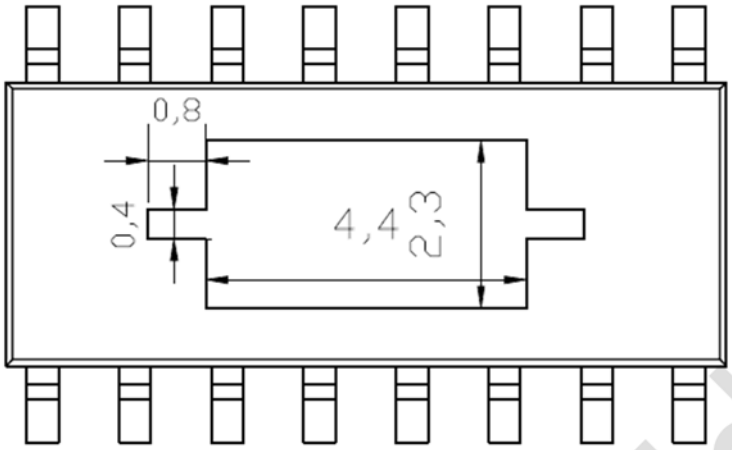
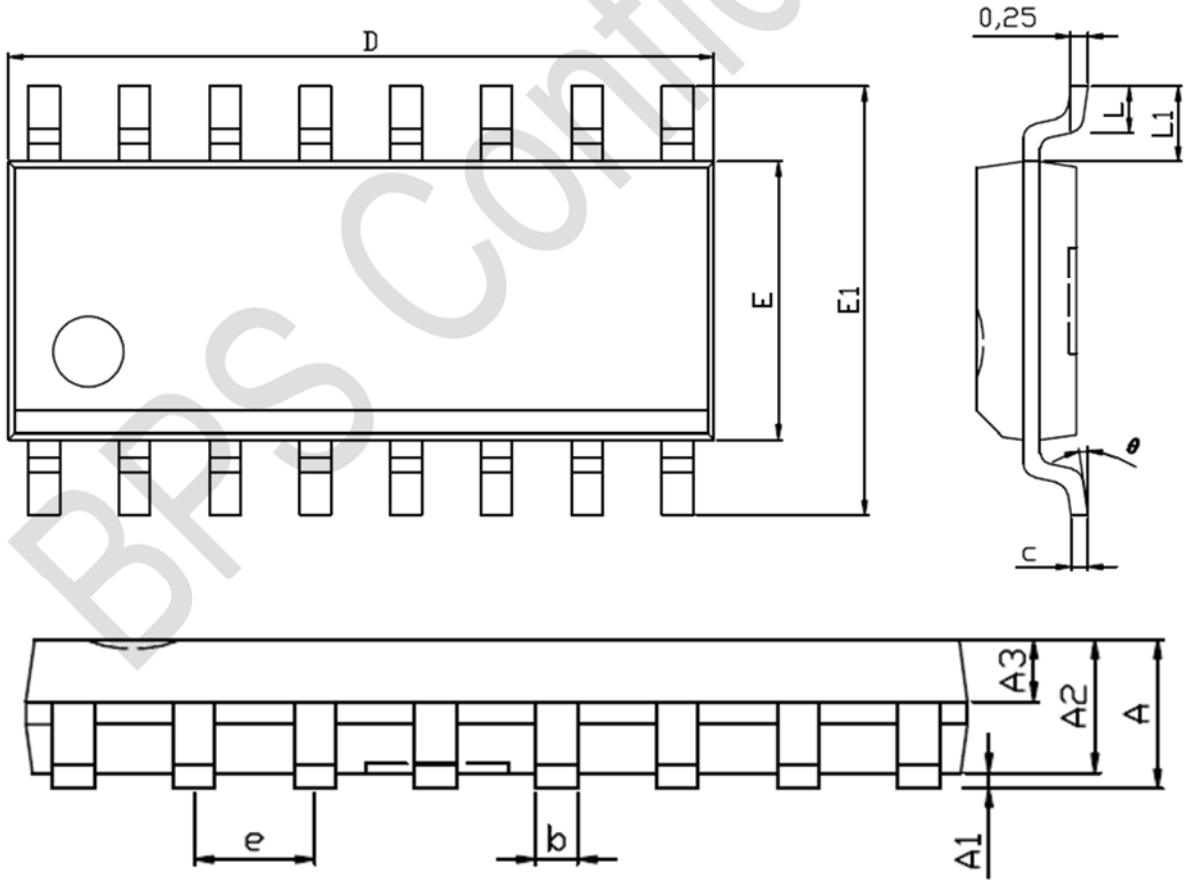
Physical Dimensions



Symbol	Dimensions In Millimeters	
	Min	Max
A		1.57
* A1	0.00	0.07
A2	1.40	1.50
A3	0.61	0.71
* b	0.39	0.45
c	0.21	0.26
D	9.70	10.10
E	3.70	4.10
* E1	5.80	6.20
* e	1.24	1.30
* L	0.60	0.80
* L1	0.99	1.10
θ	0°	8°

注1.标注“*”尺寸为测量尺寸。



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Revision Information

Revision	Date	Notes
1.0	2020-12	Initial version

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